REMARKS

Claim 51 has been amended by changing the Claim on which it depends because it correctly depends on the method of Claim 50 rather than the analogous system of Claim 18. Claim 1 has been amended by deleting the limitation "in parallel." With these amendments, the claims introduce no new matter; acceptance is respectfully requested.

There were no specific rejections of claims 34-38. However, those claims have not been rewritten into independent form because the base claim 33 should be allowed for reasons stated below.

Rejection of claims under 35 U.S.C. § 112

Claims 19, 23, 27, 44, 48, 51, 59 and 63 have been amended in response to the rejections of paragraphs 2-5 of page 2 of the subject office action. In particular, Claims 19, 23 and 51, rejected because the limitations "the delay elements" or "the parallel delay elements" lack sufficient antecedent basis, have been corrected by deleting "the," in order to introduce the limitations without prior reference. Claims 27, 44, 48, 59 and 63 have been amended by changing the claims on which they depend, so that there is sufficient antecedent basis for all limitations in these claims. With this amendment, the claims introduce no new matter; acceptance is respectfully requested.

Rejections under 35 U.S.C. §102(e) and §103(a)

Claims 1-33 and 39-66 are rejected as being unpatentable over O'Sullivan et al (US Patent 6,259,755 B1) alone or in view of Drost et al (US Patent 6,028,903). Applicant respectfully traverses those rejections and requests reconsideration.

Base Claims 1, 33 and 65 are directed to a data transmitter that controls the rise or fall transition time of a data signal, where the rise or fall transition time is the time that it takes for the data signal to change from one state to the next. As illustrated in Figure 2, an input data signal din has very short transition times from low to high and from high to low. By contrast, the data signal dout has a substantially longer transition time t_r from low to high. This long transition time is obtained by applying the data signal to parallel delay circuits as illustrated, for example, in Figures 1 and 3. The data signal output from each of those circuits has a transition time t_{r1} illustrated in

Fig. 2. However, by summing the multiple delayed signals at a common output node, it can be seen that the combined transition time of the summed signals d1'-d4' provides the longer transition t_T of signal dout (see Specification p. 7, lines 1-4). As a result, the transition time of the data output is controlled by the delayed signals, and is extended by a factor of the time td between each delayed signal.

O'Sullivan is directed to a phase-locked loop (PLL) circuit that extracts a clock signal from its random input data in a data transmission system. As shown in Figs. 6-9, data input Fdata 61 is received by both a Data Transition Detector block (DTD) 63 and a Delay Block 62. The DTD 63 outputs a "window signal" that is "high" during a short time before and after Fdata 61 changes from a low to high, as illustrated by signal 1204A in the timing diagram of Fig. 13. The window signal switches a multiplexer 68 between the voltage-controlled oscillator (VCO) 67 and a logic level (col. 6 lines 52-59), and the multiplexer 68 output is a feedback signal Ffbk 1205A. In other words the window signal allows a "window" in which the recovered clock Fclk provides feedback to the Phase Comparator Block (PCB) 64. Because time is needed to generate the window signals that control the feedback signals of the phase comparator block 64, a means of delaying the input data is required and is provided by the delay block 62 (col. 7 lines 10-13; col. 6 lines 32-36). The delay block 62 delays output for the same time required by the DTD 63 to generate a window signal, so that the data (Fref) and feedback (Ffbk) inputs are synchronized when received by the phase comparator block 64. The PCB detects the phase difference between the delayed input data 1201A and the feedback signal Ffbk 1205A (col. 6 lines 3-9). The difference in phase is output as logic 0 in the phase compared outputs 1206A and 1207A (col. 9 lines 4-9). The outputs of the Phase Comparator Block 64 then enter a charge pump 65 and low-pass filter 66 to produce a voltage output Vcnt 1208, which drives the voltage-controlled oscillator 67. Thus the Phase Comparator Block 64 controls the frequency of the recovered clock Fclk 1202 by adjusting the voltage to the voltage-controlled oscillator 67 according to a phase difference between the delayed data input and a windowed feedback signal 1205A.

Additionally, Fig. 15 of O'Sullivan discloses a way to implement the system for higher frequencies, by employing multiple delay blocks connected in series and charge pumps connected in parallel. Essentially, four circuits of the type in Figs. 6-12 receive the data input, and the charge pumps of each are combined to control a single VCO that outputs the recovered clock signal

(col.11 lines 20-26). The "first" and "second" delay circuits are connected in series to provide two different delays of the data input. The longer delay applied to the lower two circuits (PFD3/MUX3 and PFD4/MUX4) results in a delay in each PFD output. The delay causes the multiple PFD signals to change the clock in succession, resulting in a faster lock for higher-frequency data signals.

Drost was cited for a showing of parallel delay. The system of Drost is in many ways similar to O'Sullivan. It is a clock recovery system, as illustrated in Fig. 1, that outputs a clock signal in synchronization with the input data. The recovered clock signal provides a feedback signal, which is compared to the input data through a series of XOR gates and delays to maintain an accurate clock signal. As with O'Sullivan, this clock recovery system is not related to Applicant's invention. While O'Sullivan and Drost concern clock recovery of data signals, the present invention relates to transition-time control of data signals. The references teach nothing regarding controlling the transition time of signals, nor can any of the teachings of the references be used for this application. As shown in the timing diagram of Fig. 2 of Drost, all outputs and internal signals have the same high-to-low transition time as the data input. Thus, Drost is not analogous to the present invention, nor is it instructive to the problems solved by the present invention.

Applicant's data output combines delayed data signals to form a single data output, of which the rise or fall transition time is determined by these different delays. The phase comparator of O'Sullivan does not combine delayed data signals and does not determine rise or fall transition time of a data output. Rather, it detects the phase difference between a delayed data signal and a windowed clock signal. Although O'Sullivan's third example (Fig. 15) uses different delays, the delays of data signals are never combined but instead are sent to separate phase comparators. The output of the phase comparators are then applied to separate charge pumps. Only the outputs of the charge pumps, not the data signals, are combined.

In contrast, Applicant claims a combined output "wherein the rise or fall transition time of the data output is greater than the rise or fall transition time of the data input." While in O'Sullivan the input data is delayed, in Applicant's invention the input data is delayed and the transition time of the input data is extended. This distinction is illustrated by O'Sullivan Figs. 12-13 and Applicant's Figs. 1-2. O'Sullivan Fig. 12 provides two delayed data outputs (the delay

block and a data transition detector), the outputs of which are in Fig. 13 as delayed input data 1201A and retimed data 1203. Both outputs are identical to the data input, as both are shown with instantaneous transition times and are merely delayed behind the input. Applicant's Fig. 2 instead shows delayed outputs d1'-d4', which are delayed from the input data din but also have longer transition times tr, as shown by the gradual rise of each from low to high. Furthermore, the delayed outputs of O'Sullivan are never combined because the delayed input data 1201 is only sent to the phase frequency detectors 1104/1105, and the retimed data 1203 is only sent as an output. In contrast, Applicant's delayed signals d1'-d4' are combined by current drivers 129-132 to create a delayed signal dout with a gradual rise transition time that is greater than the data input, as distinctly claimed in Claim 1. Therefore, Applicant's delayed data signals are different from the delayed data signals of O'Sullivan in a distinct and nonobvious way because Applicant's delayed data signals have an extended rise or fall transition time, and these signals are combined to form a delayed output that possesses a rise or fall transition time greater than the data input. These patentable distinctions are limitations stated in independent Claims 1, 33 and 65 of the present application.

No combination of O'Sullivan and Drost teaches or suggests the invention of claims 1, 33 and 65 and their dependent claims. While Applicant claims data transmitters that control the rise or fall transition time of the data output, neither reference teaches or suggests controlling or otherwise affecting rise or fall transition time. As discussed above, transition time is not merely a matter of when a signal transitions; rather, it is a matter of the length of time for a signal to rise or fall. Delays, in the cited prior art may affect when a signal transitions. However, such delays have no effect on rise or fall transition time, nor do they suggest this effect. It is only when delayed signals are uniquely combined, as in Applicant's invention, that rise or fall transition time may be controlled. No such combination or any other transition time control is taught or suggested by the cited prior art.

Regarding Claims 18, 50 and 66, the examiner states that O'Sullivan teaches "a rise or fall transition time control for receiving and providing a controlled data signal, the transition time control controlling the transition time of the controlled signal to be proportional to bit time of the bit clock."

The rise or fall transition time control is disclosed in page 9, lines 24-29 and page 10, lines 1-29 of the present application, and illustrated in Fig. 6. The circuit of Fig. 6 may control the voltage to delay elements in Figs. 1, 3 and 5 through the output control voltage (vctrl) 151. The control voltage is controlled by the input clock 102, wherein the bit time of the clock 102 determines the control voltage 151. The rise or fall transition time of a delay element is proportional to its input voltage (vctrl). Therefore, the circuit of Fig. 6 controls a delay element so that its rise or fall transition time is proportional to the bit time of the bit clock.

No such element, or similar element, is found in O'Sullivan. As shown above regarding O'Sullivan, the Data Transition Detector (element 63, 102, 1102, 1103) outputs a "window signal" that is "high" during a short time before and after the input data 61 changes from a low to high, as illustrated by signal 1204A in the timing diagram of Fig. 13. This element does not and cannot control the rise or fall transition time of a data output, nor does it suggest this function in any way. Moreover, the bit clock (Fclk) is used by the DTD block 63 to time the "window signals" (column 7 lines 2-7). This function is entirely different from controlling the transition time of the controlled signal to be proportional to the bit time of the bit clock, as disclosed and claimed by Applicant. The bit clock in O'Sullivan has no control over the transition time of any data signal. Therefore, Applicant's base claims 18, 50 and 66 and their dependent claims are distinct from O'Sullivan in a novel and nonobvious way.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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